

CLAIMS:

We claim:

1. A semiconductor memory device compatible with an external voltage having a
5 high voltage level and a low voltage level comprising:
 - an internal voltage pad configured to connect the external voltage with an internal voltage when the external voltage is at the low voltage level;
 - an internal voltage generation circuit configured to generate the internal voltage in response to an internal voltage control signal when the external voltage is at the high voltage
10 level; and
 - an internal voltage control signal generation circuit configured to generate the internal voltage control signal according to the external voltage.
2. The semiconductor memory device of claim 1, further comprising a reference
15 voltage generation circuit configured to generate a reference voltage that stably maintains the level of the internal voltage.
3. The semiconductor memory device of claim 1, wherein the internal voltage control signal generation circuit comprises:
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 - a first control signal pad bonded to the external voltage when the external voltage is at the low voltage level;
 - a first driver for supplying a power supply voltage to the first control signal pad;
 - a second control signal pad bonded to the external voltage when the external voltage is at the high voltage level; and
 - 25 a reference voltage generation circuit for generating a reference voltage from the external voltage in response to the internal voltage control signal; and
 - an internal voltage generation circuit for comparing the reference voltage in response to the internal voltage control signal and generating an internal voltage from the external voltage.
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4. The semiconductor memory device of claim 1, wherein the internal voltage control signal generation circuit includes:
 - a fuse that is selectively shorted according to the voltage level of the external voltage;

a first PMOS transistor configured to respond to a power-up setup voltage, the first PMOS transistor being disposed between a power supply voltage and the fuse;

a first NMOS transistor configured to respond to the power-up setup signal, the first NMOS transistor being disposed between a ground voltage and the fuse;

5 an inverter chain configured to generate the internal voltage control signal in response to an output of the first NMOS transistor; and

a second NMOS transistor configured to latch the output of the first NMOS transistor in response to an output of a first inverter in the inverter chain.

10 5. A semiconductor memory device compatible with an external voltage having a high and a low voltage level, the device comprising:

an internal voltage control signal generation circuit configured to generate an internal voltage control signal according to the external voltage at the high or low voltage level;

15 a reference voltage generation circuit configured to generate a reference voltage from the external voltage in response to the internal voltage control signal; and

an internal voltage generation circuit configured to compare the external voltage with the reference voltage in response to the internal voltage control signal and configured to generate an internal voltage from the external voltage.

20 6. The semiconductor memory device of claim 5, wherein the internal voltage control signal generation circuit comprises:

a first control signal pad bonded to the external voltage when the external voltage is at the low voltage level;

25 a first driver configured to supply a power supply voltage to the first control signal pad;

a second control signal pad bonded to the external voltage when the external voltage is at the high voltage level; and

a second driver configured to supply a ground voltage to the second control signal pad.

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7. The semiconductor memory device of claim 5, wherein the internal voltage control signal generation circuit comprises:

a fuse that is selectively short-circuited according to the voltage level of the external voltage;

a first PMOS transistor configured to respond to a power-up setup voltage, the first PMOS transistor being disposed between a power supply voltage and the fuse;

a first NMOS transistor configured to respond to the power-up setup signal, the first NMOS transistor being disposed between a ground voltage and the fuse;

5 an inverter chain configured to generate the internal voltage control signal in response to an output of the first NMOS transistor; and

a second NMOS transistor configured to latch the output of the first NMOS transistor in response to an output of a first inverter in the inverter chain.

10 8. The semiconductor memory device of claim 5, wherein the reference voltage generation circuit comprises:

a PMOS transistor coupled to the external voltage and gated to the internal voltage control signal;

15 a first resistor having an end coupled to the PMOS transistor and another end coupled to the reference voltage;

a second resistor having an end coupled to the another end of the first resistor;

a first NMOS transistor coupled to another end of the second resistor and gated to the reference voltage;

20 a second NMOS transistor coupled to the first NMOS transistor and gated to the external voltage; and

a third NMOS transistor coupled to the second NMOS transistor and gated to an inverted version of the internal voltage control signal.

25 9. The semiconductor memory device of claim 5, wherein the internal voltage generation circuit comprises:

a comparator configured to compare the reference voltage with the internal voltage in response to the internal voltage control signal;

a setting unit configured to set an output of the comparator in response to the internal voltage control signal; and

30 a driver unit configured to generate the internal voltage in response to the output of the comparator.

10. An internal voltage generation circuit comprising:

a comparator configured to compare a reference voltage with an internal voltage;

a setting unit configured to set an output of the comparator in response to an enable signal;

a first driver unit configured to provide an external voltage as the internal voltage in response to the output of the comparator; and

5 a second driver unit configured to provide the external voltage as the internal voltage in response to another enable signal.

11. The internal voltage generation circuit of claim 10, wherein the enable signal and the another enable signal are activated when the external voltage is at a low voltage level.

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12. An internal voltage generation circuit comprising:

a comparator configured to compare a reference voltage with an internal voltage;

a first setting unit configured to set an output of the comparator in response to a first enable signal;

15 a second setting unit configured to set the output of the comparator after a predetermined delay in response to a second enable signal; and

a first driver unit configured to provide an external voltage as the internal voltage in response to the output of the comparator.

20 13. The internal voltage generation circuit of claim 12, wherein the first enable signal is activated when the external voltage is at a low voltage level and the second enable signal is activated when the external voltage is at a high voltage level.

14. An internal voltage generation circuit comprising:

25 a comparator configured to compare a reference voltage with an internal voltage;

a first setting unit configured to set an output of the comparator in response to a first enable signal;

a second setting unit configured to set the output of the comparator after a predetermined delay in response to a second enable signal;

30 a first driver unit configured to provide an external voltage as the internal voltage in response to the output of the comparator; and

a second driver unit configured to provide the external voltage as the internal voltage in response to a third enable signal.

15. The internal voltage generation circuit of claim 14, wherein the first and third enable signals are activated when the external voltage is at a low voltage level and the second enable signal is activated when the external voltage is at a high voltage level.

5 16. An internal voltage generation circuit comprising:
a comparator configured to compare a reference voltage with an internal voltage;
a first setting unit configured to set an output of the comparator in response to a first enable signal;
a second setting unit configured to set the output of the comparator after a
10 predetermined delay in response to a second enable signal;
a transfer unit configured to transfer the output of the comparator in response to a third enable signal;
a driver unit configured to provide an external voltage as the internal voltage in response to the output of the comparator; and
15 a second driver unit configured to provide the external voltage as the internal voltage in response to an output of the transfer unit.

17. The internal voltage generation circuit of claim 14, wherein the first and third enable signals are activated when the external voltage is at a low voltage level and the second enable signal is activated when the external voltage is at a high voltage level.

18. A method of configuring a semiconductor memory device for operation with a variable external voltage, the method comprising:
generating an internal voltage control signal according to a voltage level of the
25 external voltage;
providing the external voltage as an internal voltage when the external voltage is at a low voltage level; and
generating the internal voltage in response to the internal voltage control signal when
the external voltage is at a high voltage level.